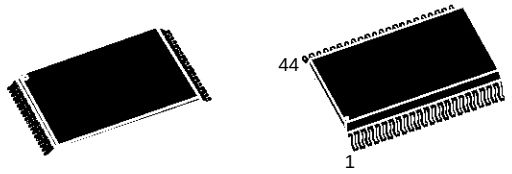
SGS-THOMSON MICROELECTRONICS

M28F841

8 Megabit (1 Meg x 8, Sector Erase) FLASH MEMORY

PRELIMINARY DATA

- SMALL SIZE PLASTIC PACKAGES TSOP40 and SO44
- MEMORY ERASE in SECTORS
  - 16 Sectors of 64K Bytes each
- 5V ± 0.5V SUPPLY VOLTAGE
- 12V ± 5% PROGRAMMING VOLTAGE
- 100,000 PROGRAM/ERASE CYCLES per SECTOR
- PROGRAM/ERASE CONTROLLER
  - Program Byte-by-Byte
  - Erase by Sector, Erase Suspend/Resume Ready/Busy Output
- LOW POWER CONSUMPTION
  - 30µA Typical in Standby
  - 0.2µA Typical in Deep Power Down
- HIGH SPEED ACCESS TIME: 100ns
- EXTENDED TEMPERATURE RANGE
- COMPATIBLE to 16 MEGABIT FLASH MEMORY
  - Equal Software Command Set
  - Pinout Compatible



TSOP40 (N)
10 x 20mm

SO44 (M)

Figure 1. Logic Diagram

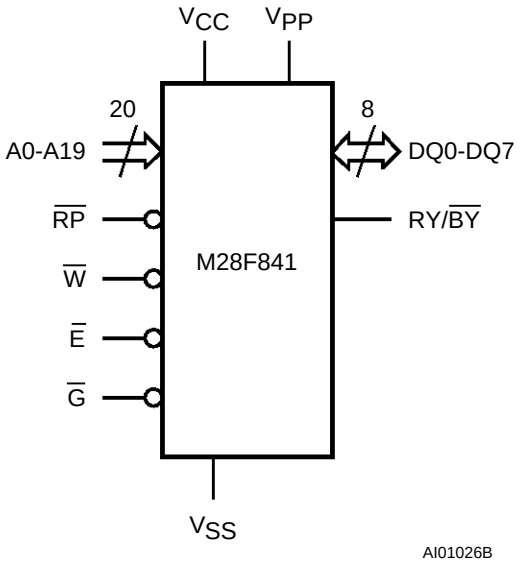
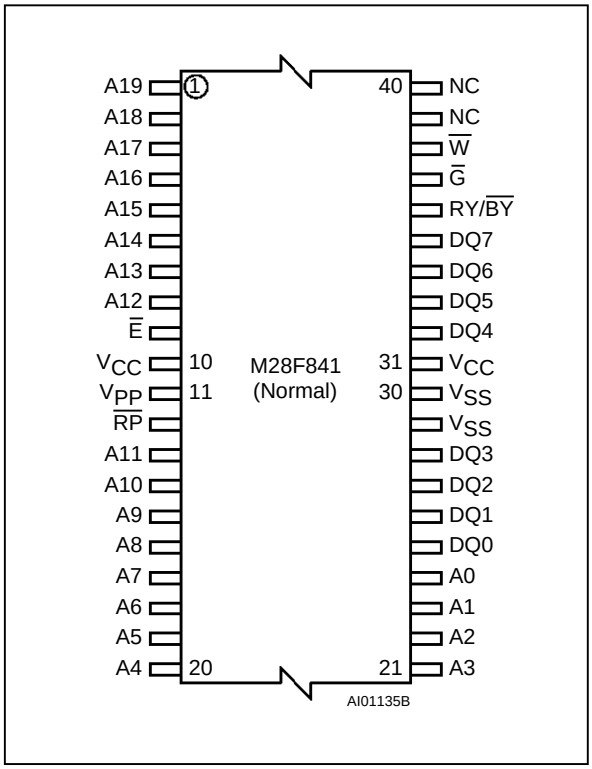


Table 1. Signal Names

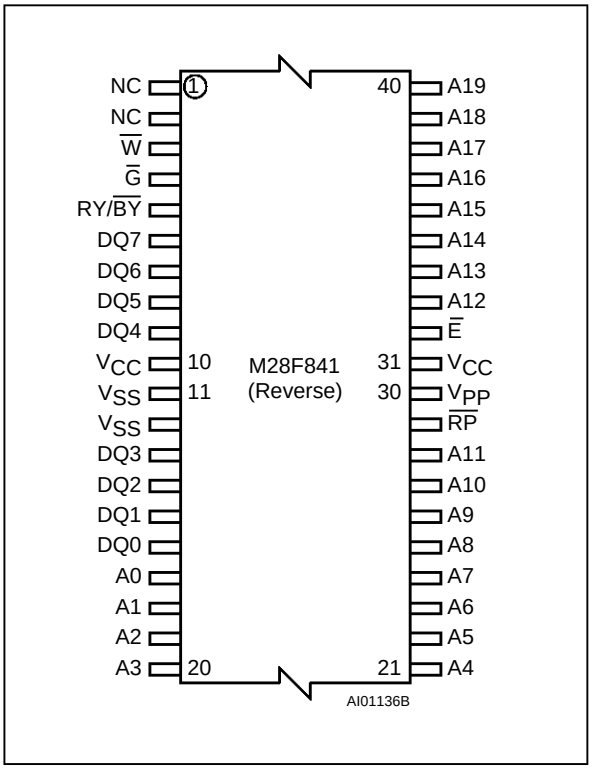
A0-A19	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Power Down
RY/$\overline{BY}$	Ready/Busy Output
V_{PP}	Program & Erase Supply Voltage
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 2A. TSOP Pin Connections



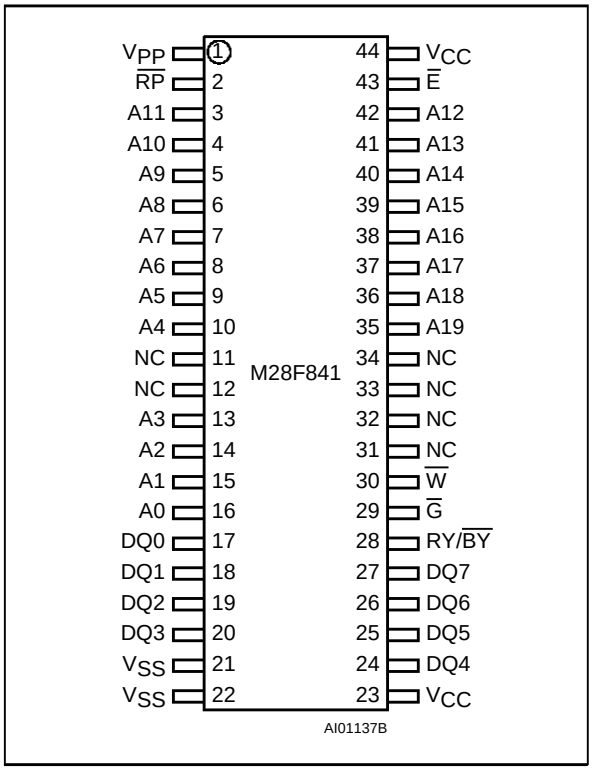
Warning: NC = Not Connected

Figure 2B. TSOP Reverse Pin Connections



Warning: NC = Not Connected

Figure 2C. SO Pin Connections



Warning: NC = Not Connected

DESCRIPTION

The M28F841 FLASH MEMORY product is a non-volatile memory that may be erased electrically at the sector level and programmed byte-by-byte. The interface is directly compatible with most microprocessors. It is intended for computer file systems and mass data storage applications. TSOP40 and S044 packages are used. The M28F841 is software and pin-out, footprint compatible with the M28V161, 16 Megabit FLASH Memory, with the simple substraction of an address line.

Organization

The organization is 1 Meg x 8 with Address lines A0-A19 and Data Input/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable inputs. A Reset/Power Down input places the memory in deep power down. A Ready/Busy output indicates the status of the internal Program/Erase Controller (P/E.C.).

Sectors

Erasure of the memory is in sectors. There are 16 sectors in the memory address space, each of 64K bytes. Programming of each sector takes typically 0.6 seconds and erasure 1.6 seconds, each sector may be programmed and erased over 100,000 cycles. All sectors are protected from programming

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature	grade 1 grade 3 grade 6	0 to 70 –40 to 125 –40 to 85	°C
T_{BIAS}	Temperature Under Bias		–50 to 125	°C
T_{STG}	Storage Temperature		–65 to 150	°C
V_{IO} (2, 3)	Input or Output Voltages		–0.6 to 7	V
V_{CC}	Supply Voltage		–0.6 to 7	V
V_{PP} (2)	Program Supply Voltage, during Erase or Programming		–0.6 to 14	V
I_{OUT} (4)	Output Short Circuit Current		100	mA

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Maximum DC voltage on I/O is V_{CC} + 0.5V, overshoot to 7V allowed for less than 20ns.
4. Only one output shorted at a time for no longer than 1 second.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	RY/$\overline{BY}$ (2)	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{OH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{OL} / V_{OH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	V_{OH}	Hi-Z
Power Down	X	X	X	V_{IL}	V_{OH}	Hi-Z

Notes: 1. X = V_{IL} or V_{IH}, V_{PP} = V_{PPL} or V_{PPH}
2. RY/$\overline{BY}$ = V_{OL} when the P/E.C. is executing a Sector Erase or Write operation. It is at V_{OH} when the P/E.C. is not busy, in the Erase Suspend or Power Down modes.

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A0	RY/$\overline{BY}$	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{OH}	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{OH}	0FCh

DESCRIPTION (cont'd)

or erasure when the Reset/Power Down $\overline{RP}$ signal is Low. Sector erase may be suspended while data is read from other sectors of the memory, then resumed.

Bus operations

Five operations can be performed by the appropriate bus cycles, Read a Byte from the Array, Output Disable, Standby, Power Down and Write a Command of an Instruction.

Command Interface

Commands can be written to a Command Interface (C.I.) latch to perform read, programming, erasure and to monitor then memory's status. When power is first applied, on exit from power down or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Memory Array.

Table 5. Instructions

Mnemonic	Instruction	Cycles	1st Cycle			2nd Cycle		
			Operation	Address (1)	Data	Operation	Address (1)	Data
RD	Read Memory Array	1+	Write	X	0FFh	Read (2)	Read Address	Data Output
RSR	Read Status Register	1+	Write	X	70h	Read (2)	X	Status Register Output
RSIG	Read Electronic Signature	3	Write	X	90h	Read (2)	Signature Adress (3)	Code Input
EE	Erase	2	Write	X	20h	Write	Sector Address	0D0h
PG	Program	2	Write	X	40h or 10h	Write	Address	Data Input
CLRS	Clear Status Register	1	Write	X	50h			
ES	Erase Suspend	1	Write	X	0B0h			
ER	Erase Resume	1	Write	X	0D0h			

Notes: 1. X = Don't Care.
2. The first cycle of the RD, RSR or RSIG instruction is followed by read operations to Read Memory Array, Read Status Register or Read Electronic Signature codes. Any number or read cycles may be performed after an RD, RSR or RSIG instructions.
3. Signature address bit A0=V_{IL} will output Manufacturer code. Address bit A0=V_{IH} will output Device code. Other address bits are ignored.

Table 6. Commands

Hex Code	Command
00h	Invalid/Reserved
10h	Alternative Program Set-up
20h	Erase Set-up
40h	Program Set-up
50h	Clear Status Register
70h	Read Status Register
90h	Read Electronic Signature
0B0h	Erase Suspend
0D0h	Erase Resume/Erase Confirm
0FFh	Read Memory Array / Reset

Instructions and Commands

Eight Instructions are defined to perform Read Memory Array, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. An internal Program/Erase Controller handles all timing and verification of the Program and Erase instructions and provides status bits to indicate its operation and exit status. Instructions are composed of a first command write operation followed by either second command write, to confirm the commands for programming or erase, or a read operation to read data from the Array, the Electronic Signature or the Status Register.

For added data protection, the instructions for byte program and sector erase consist of two commands that are written to the memory and which start the automatic P/E.C. operation. Byte programming takes typically 9µs, sector erase typically 1.6 seconds. Erasure of a memory sector may be suspended in order to read data from another sector and then resumed.

Table 7. Status Register

Mnemonic	Bit	Name	Logic Level	Definition	Note
P/ECS	7	P/E.C. Status	'1'	Ready	The RY/$\overline{BY}$ output or the P/E.C. status bit may be checked during Program or Erase. The bit should be checked on completion before checking bits b4 or b5 for success.
			'0'	Busy	
ESS	6	Erase Suspend Status	'1'	Suspended	On an Erase Suspend instruction the ESS bit is set to '1' and the P/ECS bit remains at '1'. ESS bit remains '1' until an Erase Resume instruction is given.
			'0'	In Progress or Completed	
ES	5	Erase Status	'1'	Erase Error	ES bit is set to '1' if P/E.C. has applied the maximum number of erase pulses to the block without achieving an erase verify.
			'0'	Erase Success	
PS	4	Program Status	'1'	Program Error	PS bit set to '1' if the P/E.C. has failed to program a byte or word.
			'0'	Program Success	If PS and ES bits are set to '1' during a sector erase attempt, an improper command sequence was entered and the instruction should be given again.
VPPS	3	V_{PP} Status	'1'	V_{PP} Low, Abort	VPPS bit is set if the V_{PP} voltage is below V_{PPH}(min) when a Program or Erase instruction is executed and the instruction is aborted. The Status Register must be cleared before another write or erase operation is attempted.
			'0'	V_{PP} OK	
	2	Reserved			Bits b2, b1 and b0 are reserved for future use and should be masked out when polling the Status Register.
	1	Reserved			
	0	Reserved			

Note: Logic level '1' is High, '0' is Low.

A Status Register may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. In addition a Ready/Busy output RY/$\overline{BY}$ indicates the status of the P/E.C. After Programming or Erasure the command interface must be reset by giving the Read Memory Array instruction before the memory contents can be accessed.

Power Saving

The M28F841 memory have a number of power saving features. A CMOS standby mode is entered when the Chip Enable $\overline{E}$ and the Reset/Power Down $\overline{RP}$ signals are at V_{CC}, when the supply current drops to typically 30µA. A deep power down mode is enabled when the Reset/Power Down signal $\overline{RP}$ is at V_{SS}, when the supply current drops to typically 0.2µA. The time required to awake from the deep power down mode is 1µs maximum, with instructions to the C.I. recognized after 400ns.

AC MEASUREMENT CONDITIONS

Input Rise and Fall Times	≤ 10ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Input Output Waveforms

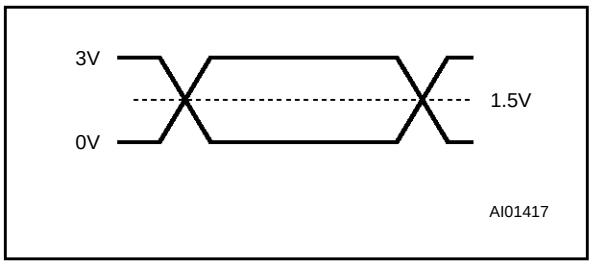


Figure 4. AC Testing Load Circuit

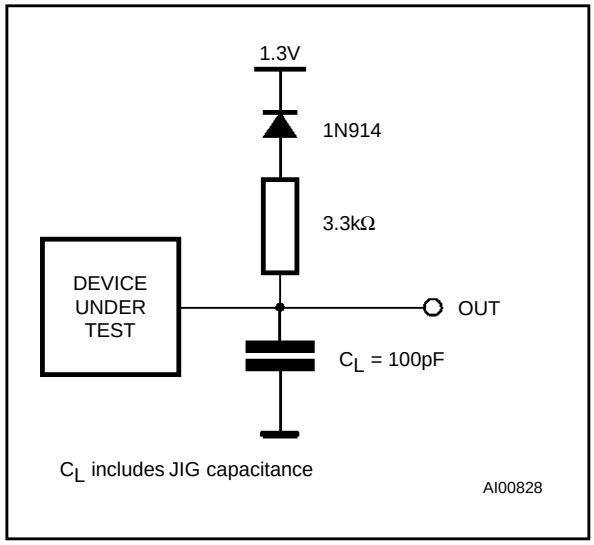


Table 8. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

DEVICE OPERATION

Signal Descriptions

A0-A19 Address Inputs. The address signals, inputs for the memory array, are latched during a write operation.

DQ0-DQ7 Data Input/Outputs. The data inputs, a byte to be programmed or a command to the C.I., are latched on the rising edge of Chip Enable $\overline{E}$ and Write Enable $\overline{W}$, whichever occurs first. The data output from the memory Array, the Electronic Signature or the Status Register is valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

$\overline{E}$ Chip Enable. The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High de-selects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the C.I. and the memory Array while $\overline{W}$ remains at a low level. Both addresses and data inputs are then latched on the rising edge of $\overline{E}$.

$\overline{RP}$ Reset/Power Down. This input allows the memory to be placed in a deep power down mode. If $\overline{RP}$ is within V_{SS} ± 0.2V the lowest supply current is absorbed.

RY/$\overline{BY}$ Read/Busy. This output indicates when the Program Erase Controller is executing a program or erase. It is always active, even during power down. If RY/$\overline{BY}$ is at V_{OL}, the P/E.C. is active.

$\overline{G}$ Output Enable. The Output Enable gates the outputs through the data buffers during a read operation.

$\overline{W}$ Write Enable. This controls writing to the C.I., Address and Input Data latches. Both Addresses and Input Data are latched on the rising edge of $\overline{W}$.

V_{PP} Program Supply Voltage. This supply voltage is used for memory Programming and Erase.

V_{CC} Supply Voltage. This is the main circuit supply.

V_{SS} Ground. This is the reference for all the voltage measurements.

Table 9. DC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±10	µA
I_{CC} (1, 3)	Supply Current (Read) TTL	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$, f = 8MHz		30	mA
	Supply Current (Read) CMOS	$\overline{E} = V_{SS}$, $\overline{G} = V_{SS}$, f = 8MHz		20	mA
I_{CC1} (1, 3)	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$, $\overline{RP} = V_{IH}$		1	mA
	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		100	µA
I_{CC2} (1, 3)	Supply Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{CC3} (1, 3)	Supply Current (Program)	Byte program in progress		30	mA
I_{CC4} (1, 3)	Supply Current (Erase)	Sector Erase in progress		30	mA
I_{CC5} (1, 2, 3)	Supply Current (Erase Suspend)	$\overline{E} = V_{IH}$, Erase suspended		6	mA
I_{PP}	Program Current (Read)	$V_{PP} > V_{CC}$		200	µA
I_{PP1}	Program Current (Standby)	$V_{PP} \le V_{CC}$		±10	µA
I_{PP2}	Program Current (Power Down)	$\overline{RP} = V_{SS} \pm 0.2V$		5	µA
I_{PP3}	Program Current (Program)	Byte program in progress		15	mA
I_{PP4}	Program Current (Erase)	Sector Erase in progress		10	mA
I_{PP5}	Program Current (Erase Suspend)	Erase suspended		200	µA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –2mA	2.4		V
V_{PPL}	Program Voltage (Normal operation)		0	V_{CC} + 0.5	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4	12.6	V
V_{LKO}	Supply Voltage (Program or Erase Lock-out)		2		V

Notes: 1. Supply Current specified with I_{OUT} ($RY/\overline{BY}$) = 0.
2. Current increases to I_{CC} + I_{CC5} during a read operation with erase suspended.
3. CMOS levels V_{CC} ± 0.2V and V_{SS} ± 0.2V. TTL levels V_{IH} and V_{IL}.

Memory Sectors

There are 16, 64K Byte memory sectors. Each sector of the memory can be erased separately, but only one sector at a time. The erase operation is managed by the P/E.C. but can be suspended in order to read from another sector and then resumed.

Programming and erasure of the memory is disabled when the Program Supply Voltage is at V_{PPL}. For successful programming and erasure the Program Supply Voltage must be at V_{PPH} throughout the operation.

Table 10. Read AC Characteristics
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	Test Condition	M28F841						Unit
				-100		-120		-150		
				Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	100		120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		100		120		150	ns
t_{PHQV}	t_{PWH}	Power Down High to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		1		1		1	µs
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		100		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		45		50		50	ns
t_{EHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		50		50		55	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		40		50	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Operations

Operations are defined as specific bus cycles and signals which allow memory Read, Command Write, Output Disable, Standby, Power Down and Electronic Signature Read. They are shown in Table 3.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be Low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. A read operation will output a byte on DQ0-DQ7.

The data read depends on the previous command written to the C.I. (see instructions RD, RSR and RSIG).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Commands, Input Data and Addresses are latched on the rising edge of $\overline{W}$ or $\overline{E}$. As for read operations data is transferred on DQ0-DQ7.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Figure 5. Read Mode AC Waveforms

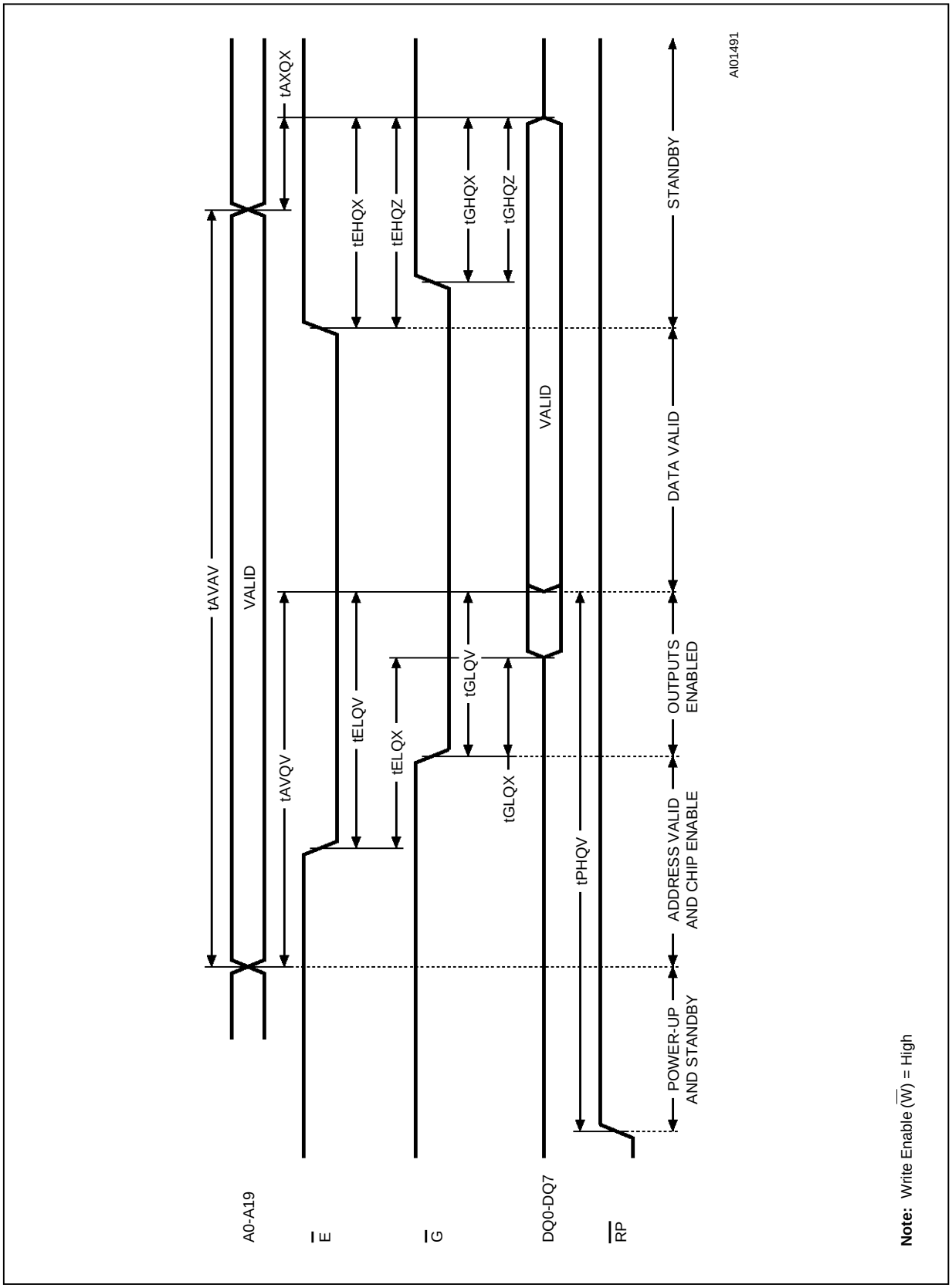


Table 11. Byte Program, Erase Time
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V)

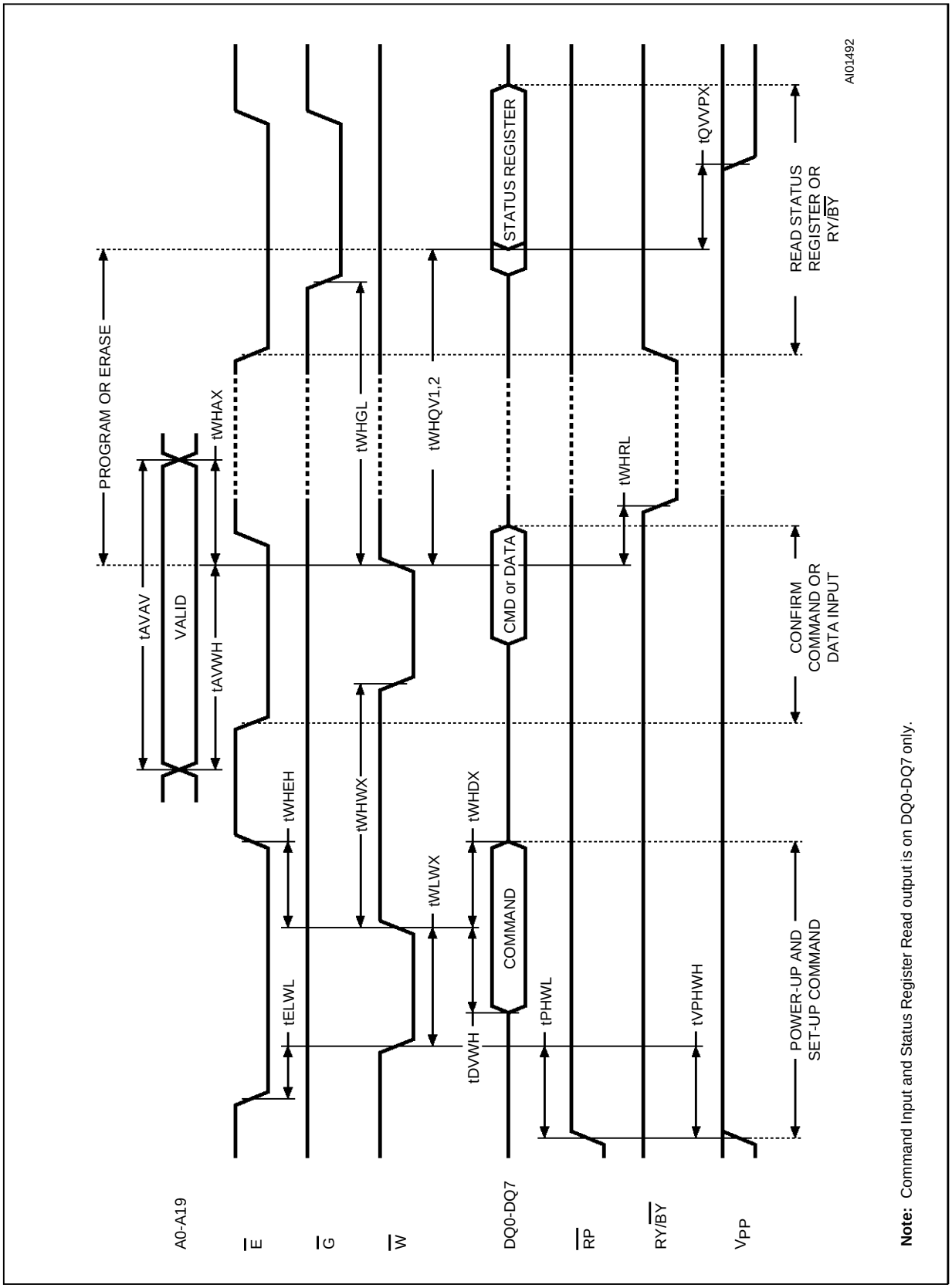
Parameter	Test Conditions	M28F841			Unit
		Min	Typ	Max	
Block Program	V_{PP} = 12V ± 5%		0.6	2.1	sec
Block Erase	V_{PP} = 12V ± 5%		1.6	10	sec

Table 12. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F841						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHWL} (1)	t_{PS}	Power Down High to Write Enable Low	1		1		1		µs
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		0		ns
t_{WLWX}	t_{WP}	Write Enable Low to Write Enable Transition	40		40		40		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	40		40		40		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	5		5		5		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	10		10		10		ns
t_{WHWX}	t_{WPH}	Write Enable High to Write Enable Transition	30		30		30		ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	40		40		40		ns
t_{VPHWH} (1)	t_{VPS}	V_{PP} High to Write Enable High	100		100		100		ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	5		5		5		ns
t_{WHGL}		Write Enable High to Output Enable Low	0		0		0		ns
t_{WHRL}		Write Enable High to Ready Busy Low		100		100		100	ns
t_{WHQV1} (2)		Write Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{WHQV2} (2, 3)		Write Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 6. Program & Erase AC Waveforms, $\overline{W}$ Controlled



Note: Command Input and Status Register Read output is on DQ0-DQ7 only.

Table 13. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, -40 to 85°C or -40 to 125°C; V_{CC} = 5V ± 0.5V; V_{PP} = 12V ± 5%)

Symbol	Alt	Parameter	M28F841						Unit
			-100		-120		-150		
			Min	Max	Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	100		120		150		ns
t_{PHEL} (1)	t_{PS}	Power Down High to Chip Enable Low	1		1		1		µs
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		0		ns
t_{ELEX}	t_{CP}	Chip Enable Low to Chip Enable Transition	50		50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	40		40		40		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	5		5		5		ns
t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	5		5		5		ns
t_{EHEX}	t_{EPH}	Chip Enable High to Chip Enable Transition	25		25		25		ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	40		40		40		ns
t_{VPHEH} (1)	t_{VPS}	V_{PP} High to Chip Enable High	100		100		100		ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	5		5		5		ns
t_{EHGL}		Chip Enable High to Output Enable Low	0		0		0		ns
t_{EHRL}		Chip Enable High to Ready Busy Low		100		100		100	ns
t_{EHQV1} (2)		Chip Enable High to Output Valid (Byte Program)	6		6		6		µs
t_{EHQV2} (2, 3)		Chip Enable High to Output Valid (Sector Erase)	0.3		0.3		0.3		sec
t_{QVVPX} (1, 2)	t_{VPH}	Output Valid or Ready Busy High to V_{PP} Transition	0		0		0		ns

Notes: 1. Sampled only, not 100% tested.
2. Byte Program and Sector Erase durations are measured to completion as indicated by Status Register b7 = 1 or RY/$\overline{BY}$ = high. V_{PP} is held high until Status Register bits b3, b4 and b5 indicate Program or Sector Erase success.
3. Temperature range 0 to 70 °C (grade 1) only.

Figure 7. Program & Erase AC Waveforms, $\overline{E}$ Controlled

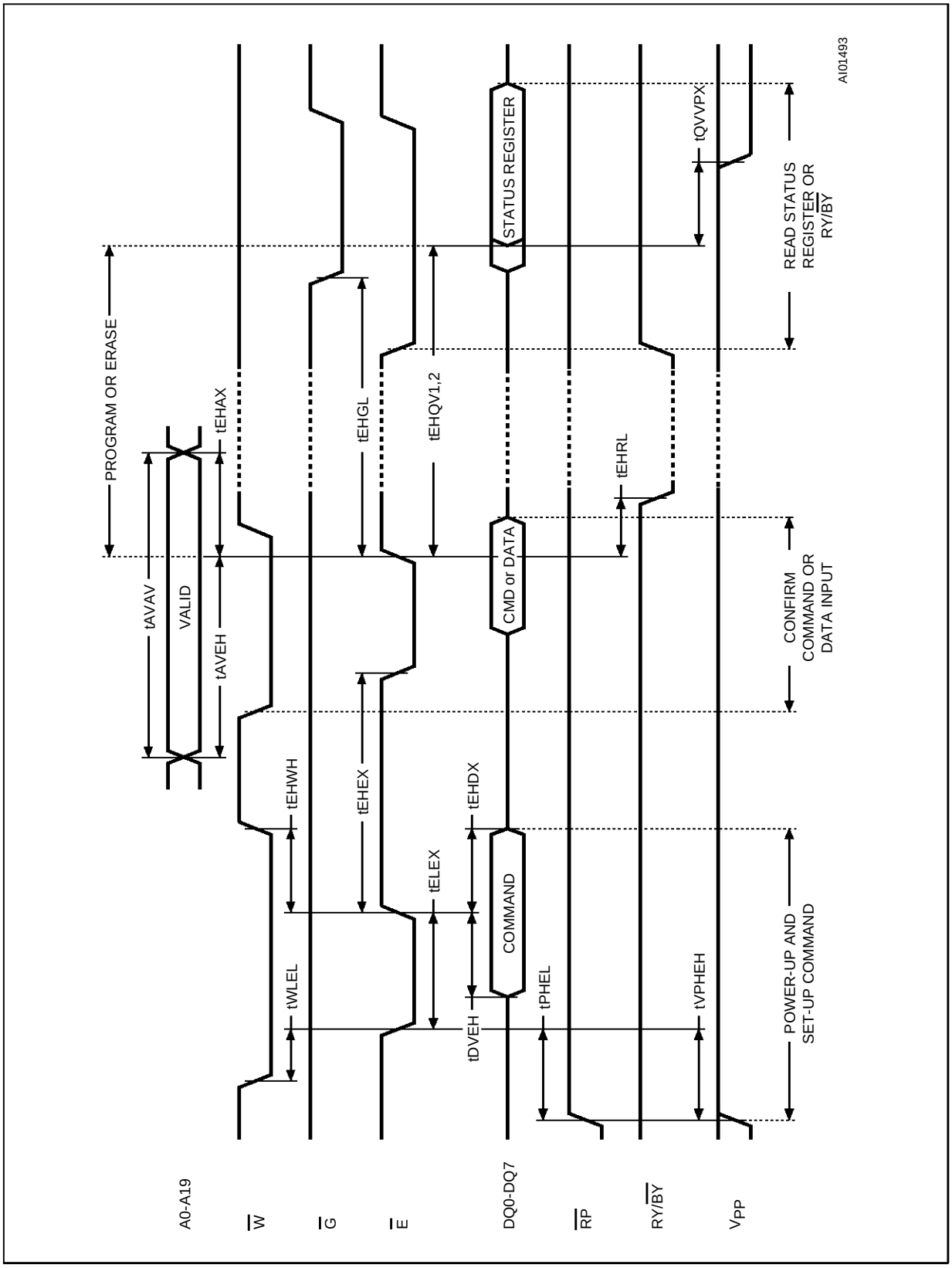
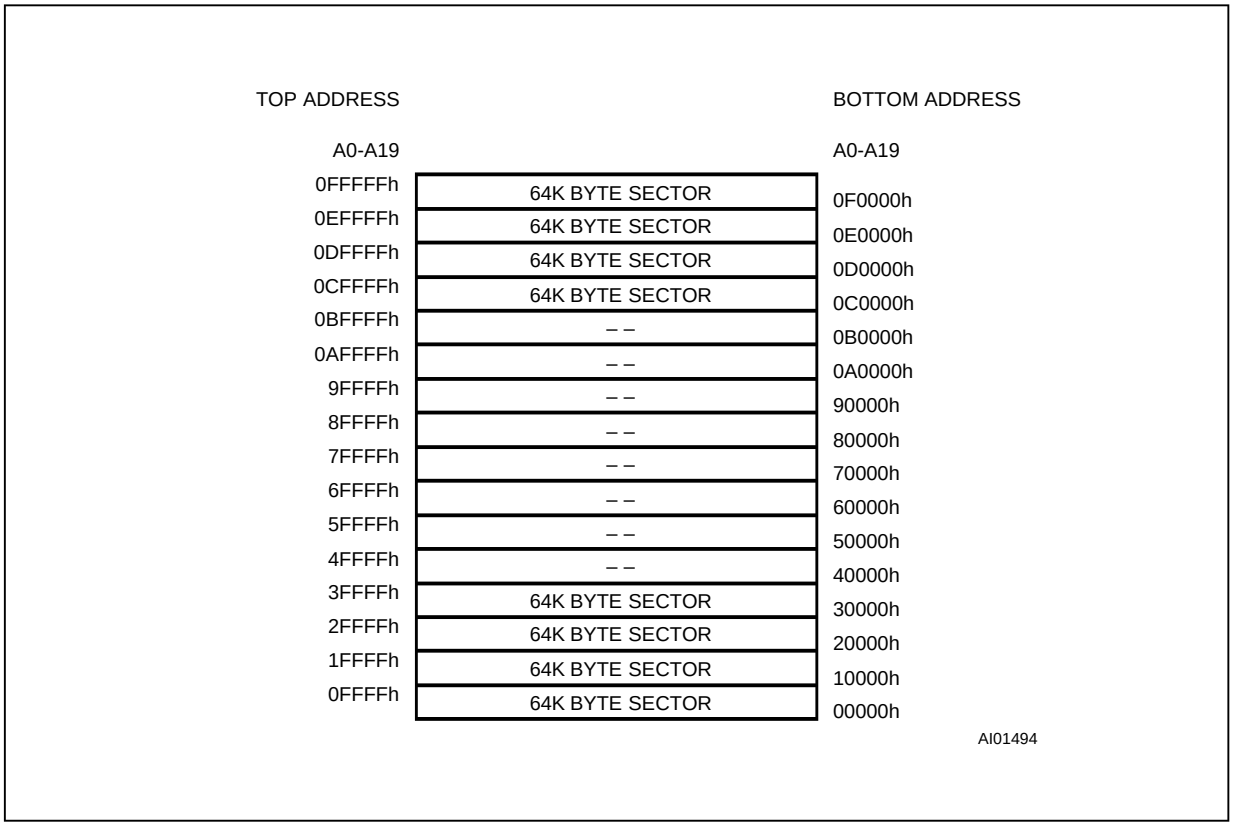


Figure 8. Memory Map, Byte-wide Addresses



Standby. The memory is in standby when the Chip Enable $\overline{E}$ is High. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Power Down. The memory is in Power Down when $\overline{RP}$ is Low. The power consumption is reduced to the power down level and the outputs are high impedance independent of the Chip Enable $\overline{E}$, Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory, the manufacturer code for SGS-THOMSON is 20h and the device code for the M28F841 is 0FCh. These codes allow applications to match their interfaces to the characteristics of the particular manufacturer's product.

The two Electronic Signature codes are output by a read operations with the Address line A0 at V_{IL} or V_{IH}, following an instruction RSIG to the memory.

Instructions and Commands

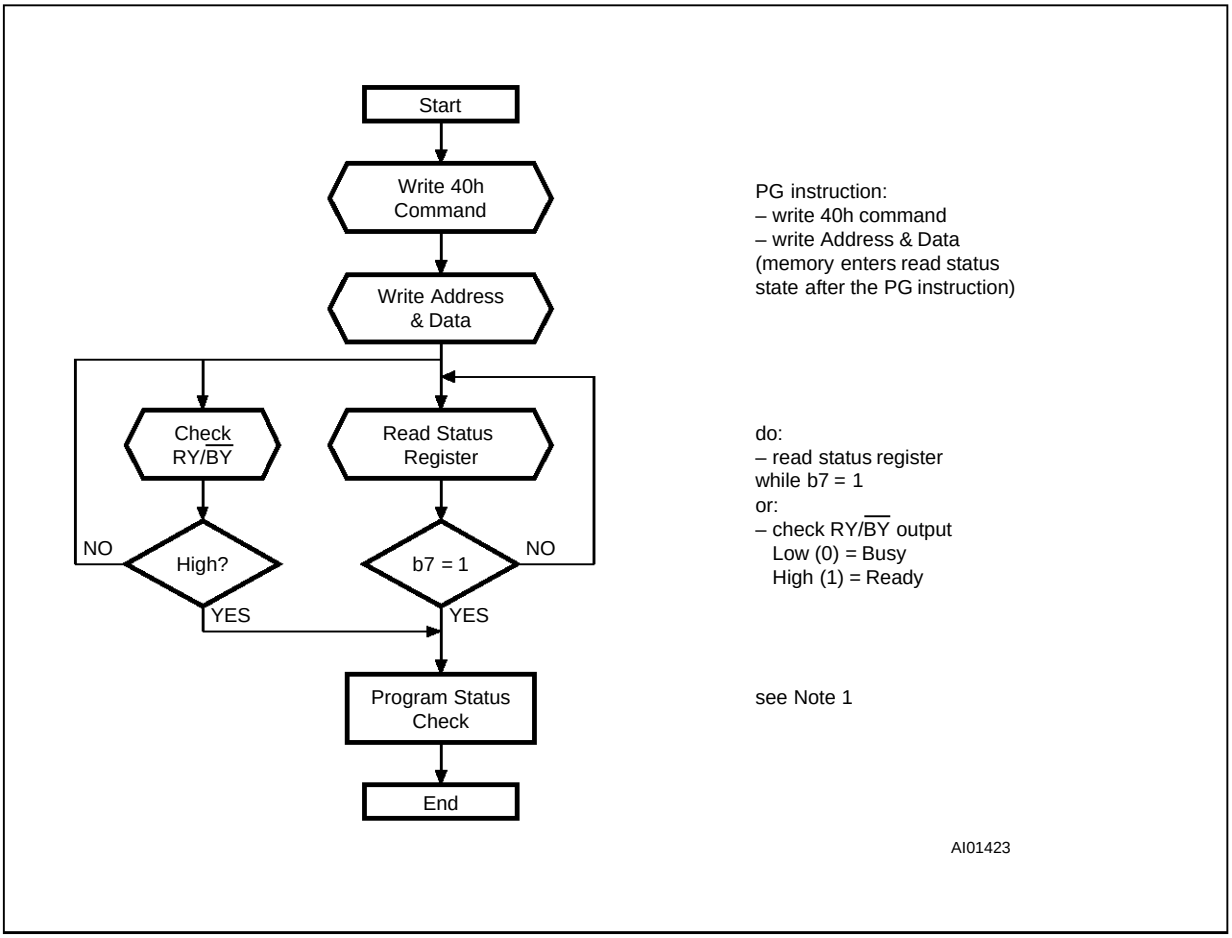
The memory includes a Command Interface (C.I.) which latches commands written to the memory. Instructions are made up from one or more commands to perform memory Read, Read Status Register, Read Electronic Signature, Erase, Program, Clear Status Register, Erase Suspend and Erase Resume. These instructions require from one to 3 operations, the first of which is always a write operation followed by either a further write operation to input address and data or to confirm the command, or a read operation to output data.

A Status Register indicates the P/E.C. status Ready/Busy, the suspend/in-progress status of erase operations, the failure/success of erase and program operations and the low/correct value of the V_{PP} Program Supply Voltage.

The P/E.C. sets status bits b3 to b7 and clears bit b6 & b7. It cannot clear bits b3 to b5. The status register can be read by the Read Status Register RSR instruction and cleared by the Clear Status Register CLRS instruction. The meaning of the register bits b3 to b7 is shown in Table 7. Bit b0 to b2 are reserved for future use and should be masked out during status checks.

The P/E.C. Ready/Busy status is also indicated by the RY/$\overline{BY}$ output.

Figure 9. Program Flow-chart and Pseudo Code



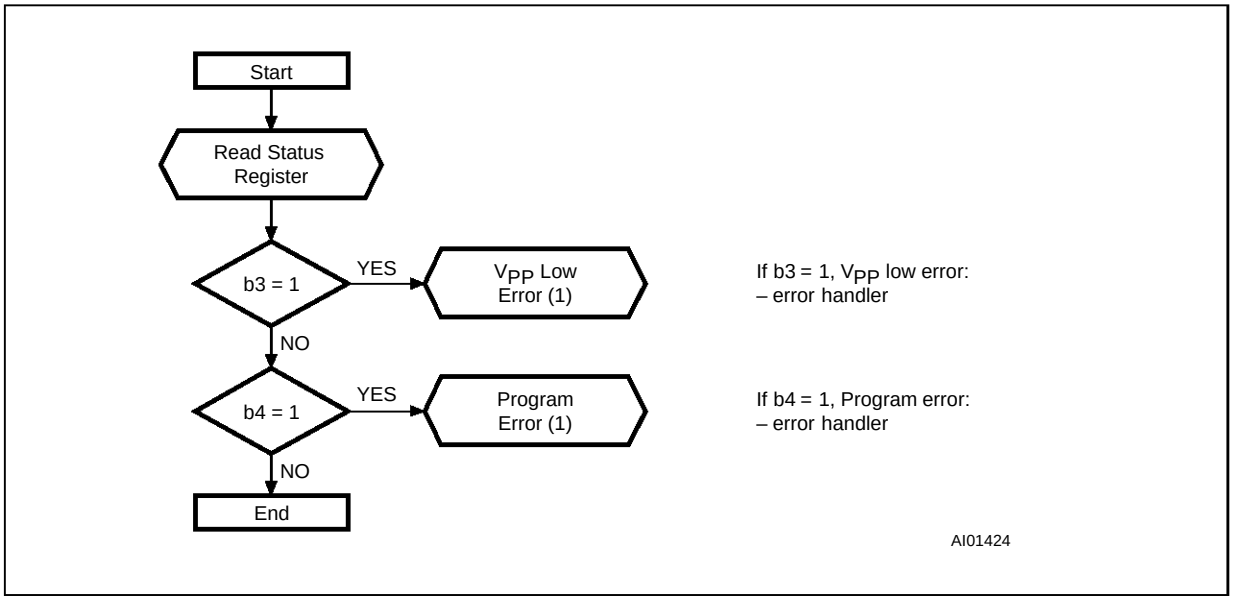
Note: 1. Status check of b7 can be made after each byte programming or after a sequence.

Read (RD) instruction. The Read instruction consists of one write operation giving the command 0FFh. Subsequent read operations will read data from the addressed byte of the memory array, until a new command is written to the C.I.

Read Status Register (RSR) instruction. The Read Status Register instruction may be given at any time, including while the Program/Erase Controller is active. It consists of one write operation giving the command 70h. Subsequent read operations output the contents of the status register. The contents are latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to its initial high level. Either $\overline{E}$ or $\overline{G}$ must be toggled to V_{IH} to update the latch. Additionally, any read attempt during program or erase operation will automatically output the contents of the status register.

Read Electronic Signature (RSIG) instruction. This instruction uses 3 operations. It consists of one write operation giving the command 90h, followed by two read operations to output the manufacturer and device codes. The manufacturer code is output when the address line A0 is Low and the device code when A0 is High.

Figure 10. Program Status Check Flow-chart and Pseudo Code



Note: 1. If a V_{PP} Low or Program error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Erase (EE) instruction. The memory can be erased in sectors. The Program Supply Voltage V_{PPH} must be applied before the Erase (EE) instruction is given. This instruction uses two write operations. The first command written is the Erase Set-up command 20h. The second is the Erase Confirm command 0D0h. During the input of the second command an address within the sector to be erased is given and this is latched into the memory. If the second command given is not the Erase Confirm command then the status register bits b4 & b5 are set and the instruction aborts. Read operations output the status register after erasure has started.

During the execution of the erase by the P/E.C., the memory accepts only the Read Status Register (RSR) or Erase Suspend (ES) instructions. Status Register bit b7 returns '0' while the erasure is in progress and '1' when it is completed. After completion the Status Register bit b5 returns '1' if there has been an erase failure because erasure has not been verified after even the maximum number of erase pulses have been given. The Status Register bit b3 returns '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when erasure is attempted and/or proceeding.

V_{PP} must be at V_{PPH} when erasing. Erase should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. If V_{PP} falls below V_{PPH} or if $\overline{RP}$ goes Low the erase aborts and must be repeated, after having cleared the Status Register with the CLRS instruction.

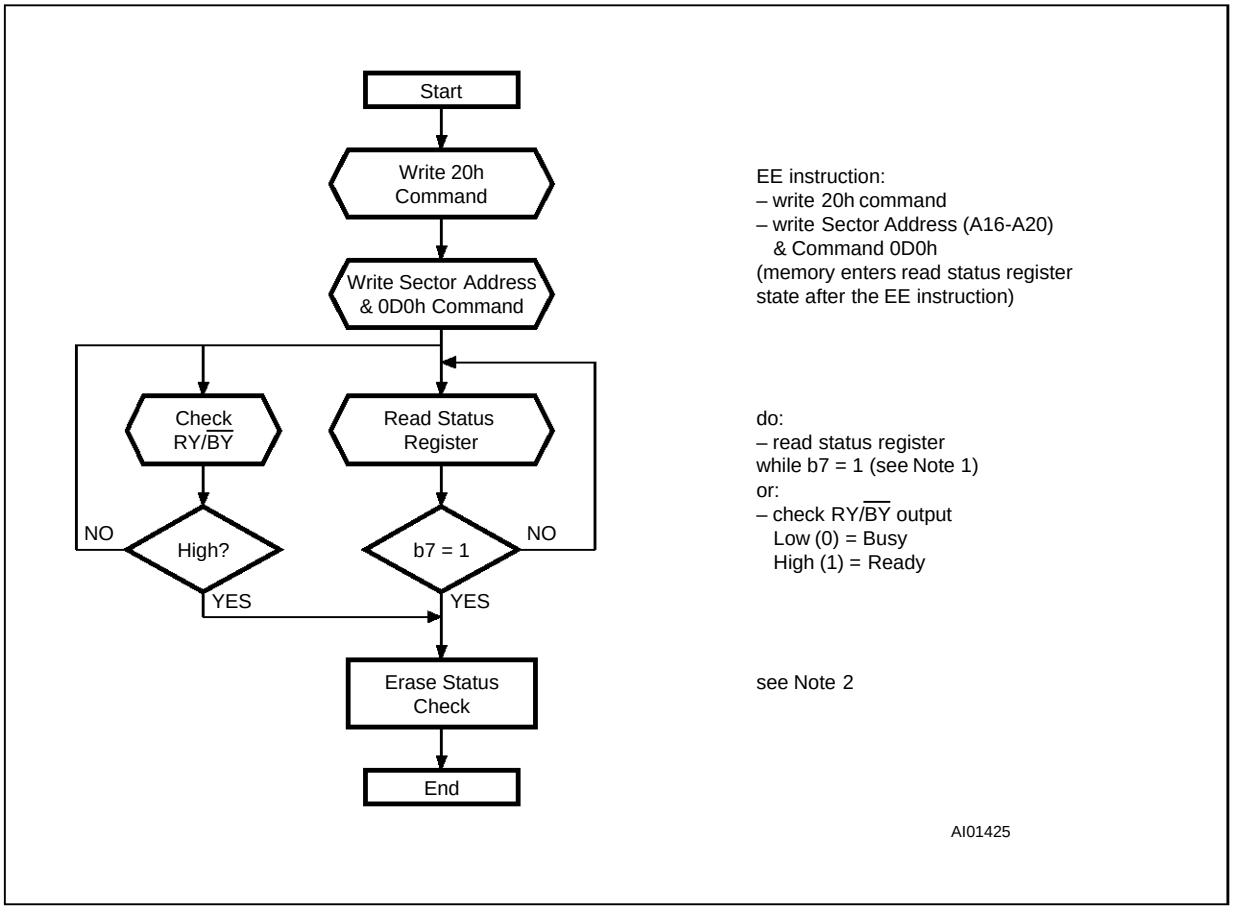
The execution of the erase by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

A full status check can be made after sector erase. The status check is made on the Status Register bit b3 for any possible V_{PP} error, on bit b5 for an erase error or on both bits b4 & b5 for a command sequence error.

Program (PG) instruction. The memory is programmed byte-by-byte. The Program Supply Voltage V_{PPH} must be applied before the Program (PG) instruction is given and may be applied continuously during programming of a sequence of bytes. This instruction uses two write operations. The first command written is the Program Set-up command 40h (or alternatively 10h). A second write operation latches the address and input data and starts the P/E.C. execution. Read operations output the Status Register after programming has started.

Memory programming is only made by writing a '0' in place of a '1' in a byte. To write a '1' in place of a '0' the Sector must first be erased to all '1's.

Figure 11. Erase Flow-chart and Pseudo Code



Notes: 1. An Erase Suspend may be executed during this loop.
2. See separate flow-chart.

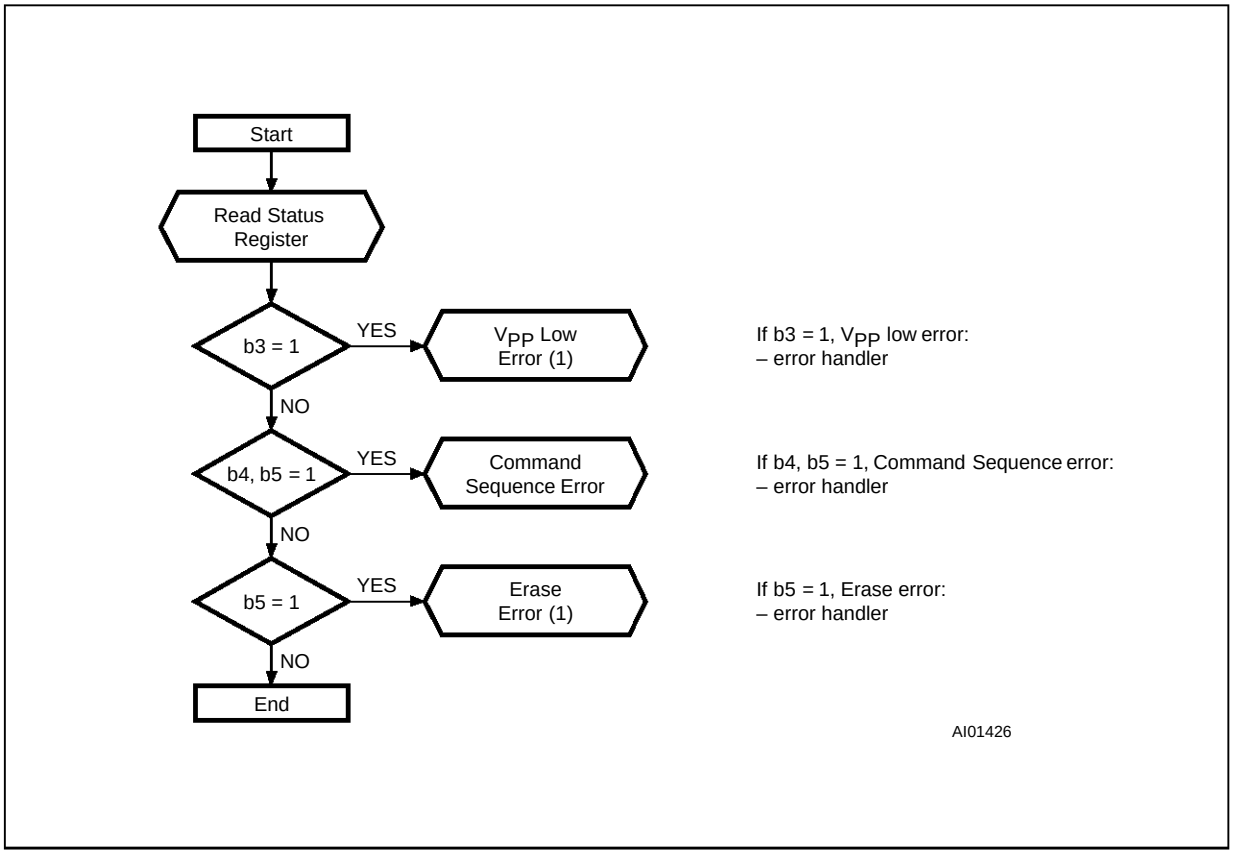
During the execution of the programming the memory accepts only the Read Status Register (RSR) instruction. The Status Register bit b7 returns '0' while programming is in progress and '1' when it is completed. After completion the Status Register bit b4 returns '1' if there has been a program failure. Status Register bit b3 returns a '1' if the Program Supply Voltage V_{PP} does not remain at V_{PPH} when programming is attempted and/or during programming.

V_{PP} must be at V_{PPH} when programming. Programming should not be attempted when $V_{PP} < V_{PPH}$ as the results will be uncertain. Programming aborts if V_{PP} drops below V_{PPH} or $\overline{RP}$ goes Low. If aborted the data may be incorrect, the Status Register must be cleared with the Clear Status Register (CLRS) instruction, the sector erased and reprogrammed.

The execution of the programming by the P/E.C. is also indicated by the RY/$\overline{BY}$ output.

A full status check can be made after each byte or after a sequence of bytes has been programmed. The status check is made on the Status Register bit b3 for any possible V_{PP} error and on bit b4 for a programming error.

Figure 12. Erase Status Check Flow-chart and Pseudo Code



Note: 1. If V_{PP} Low or Erase error is found, the Status Register must be cleared (CLRS instruction) before further P/E.C. operations.

Clear Status Register (CLRS) instruction. This instruction uses a single write operation which clears the Status Register bits b3, b4 & b5 to '0'. The CLRS instruction reverts the device to the Read Array mode and is used before any new operation when errors have been detected during programming or erasure.

Erase Suspend (ES) instruction. An Erase operation may be suspended by using this instruction which consists of writing the command 0B0h. The Status Register bit b6 indicates wether the P/E.C. is suspended, bit b6 = '1', or whether the P/E.C. cycle was the last and the erase is complete, bit b6 = '0'. During suspension the memory will respond only to Read (RD), Read Status Register (RSR) or Erase Resume (ER) instructions. Immediately following the ES instruction, read operations initially output the contents of the Status Register while erase is suspended, but if a Read (RD) instruction is given data may be read from other sectors of the memory. The Program Supply Voltage V_{PP} must be maintained at V_{PPH} while erase is suspended. If V_{PP} does not remain at V_{PPH} or if the $\overline{RP}$ input goes Low, the erase operation is aborted and Status Register bits b3 & b5 are set. In this case the Status Register must be cleared and the erase operation repeated to be certain to erase the sector.

Erase Resume (ER) instruction. If an Erase Suspend instruction has been previously executed, the erase operation may be resumed giving the command 0D0h. The Status Register bit b6 will be cleared when erase resumes. Read operations output the Status Register after the erase is resumed.

Reset. After any error has occurred during programming or erase the Status Register must be cleared by giving the Clear Status Register instruction before the memory array may be read.

After a successful program or erase operation either the Read or Clear Status Register instruction must be given before the memory array may be read.

Figure 13. Erase Suspend & Resume Flow-chart and Pseudo Code

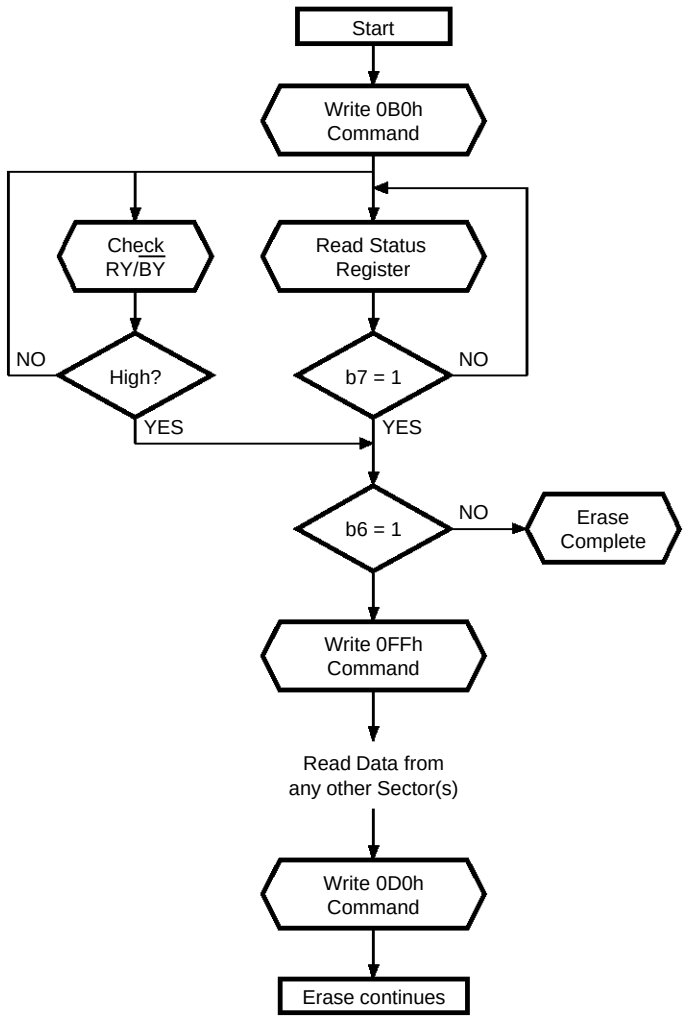
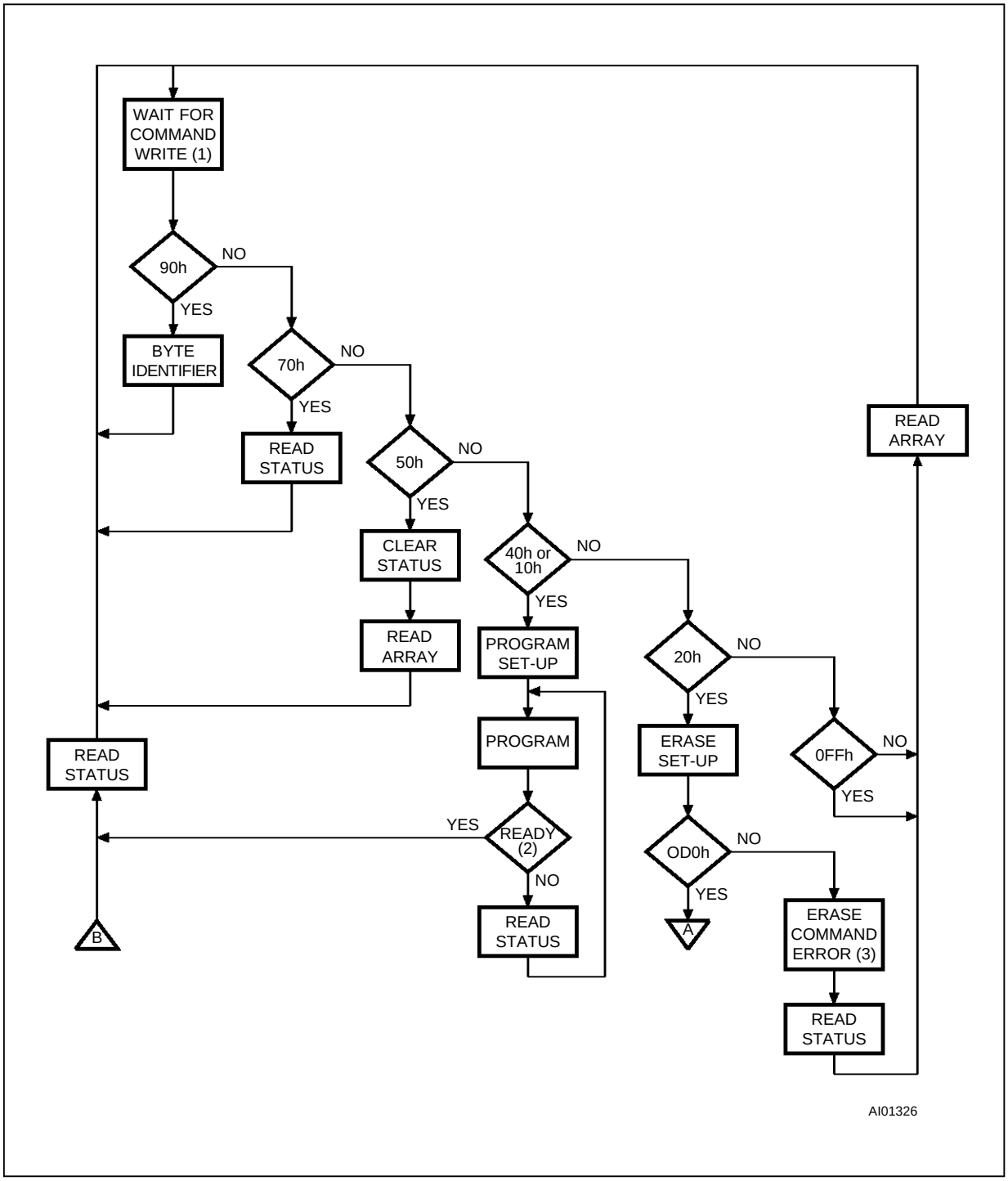
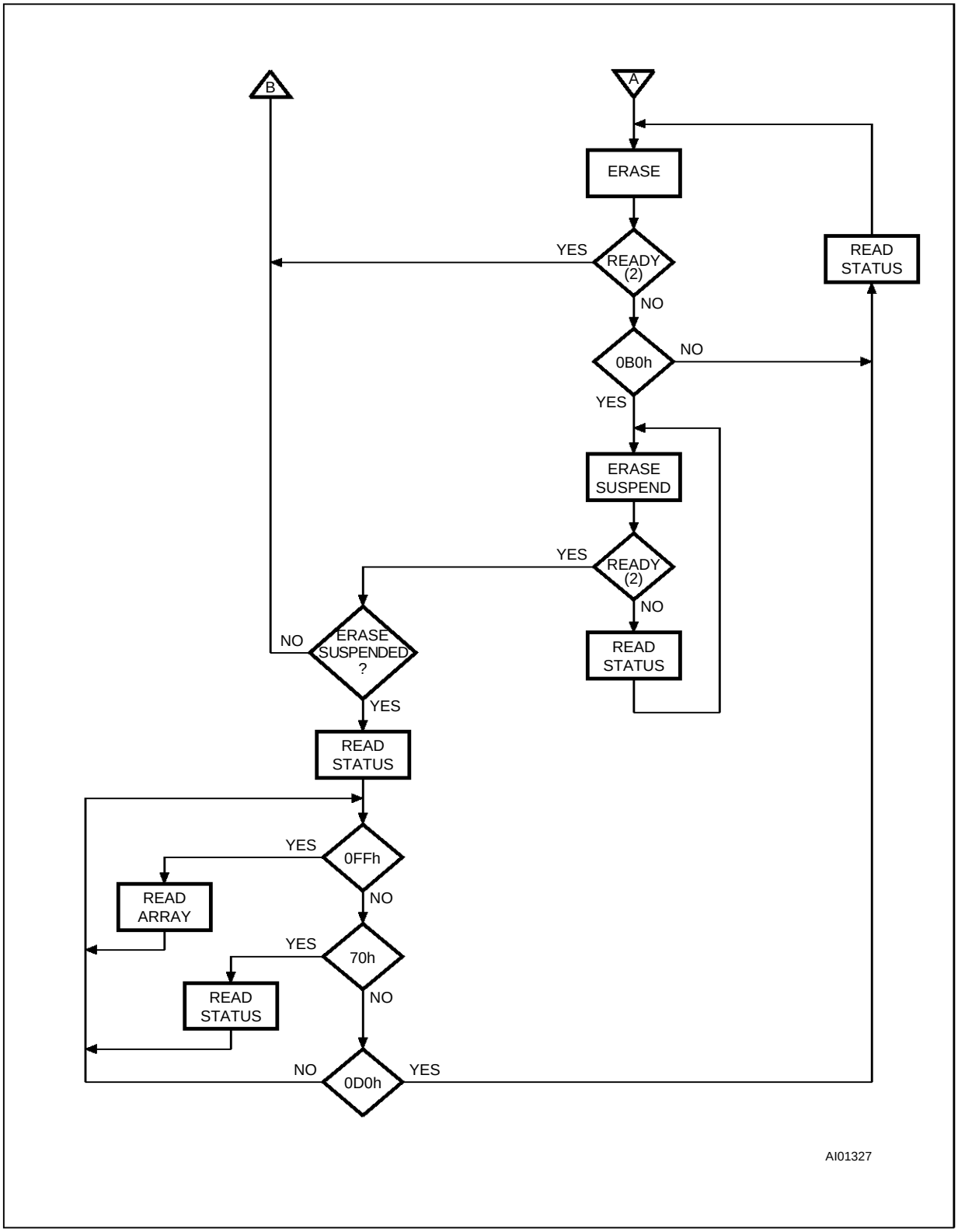


Figure 14. Command Interface and Program Erase Controller Flow-diagram (a)



Notes: 1. If no command is written, the Command Interface remains in its previous valid state. Upon power-up, on exit from power-down or if V_{CC} falls below V_{LKO}, the Command Interface defaults to Read Array mode.
2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.
3. Upon Erase command error, the P/E.C. defaults to Read status and sets bits b4 and b5 of the Status Register. Program and Erase commands will be accepted only after the Status Register has been reset by a CLRS command.

Figure 15. Command Interface and Program Erase Controller Flow-diagram (b)



Note: 2. P/E.C. status (Ready or Busy) is read on Status Register bit 7.

ORDERING INFORMATION SCHEME

Example: M28F841 -100 N 1 TR

Speed		Package		Temp. Range		Option	
-100	100ns	M	SO44	1	0 to 70 °C	R	Reverse Pinout
-120	120ns	N	TSOP40 10 x 20mm	3	–40 to 125 °C	TR	Tape & Reel Packing
-150	150ns			6	–40 to 85 °C		

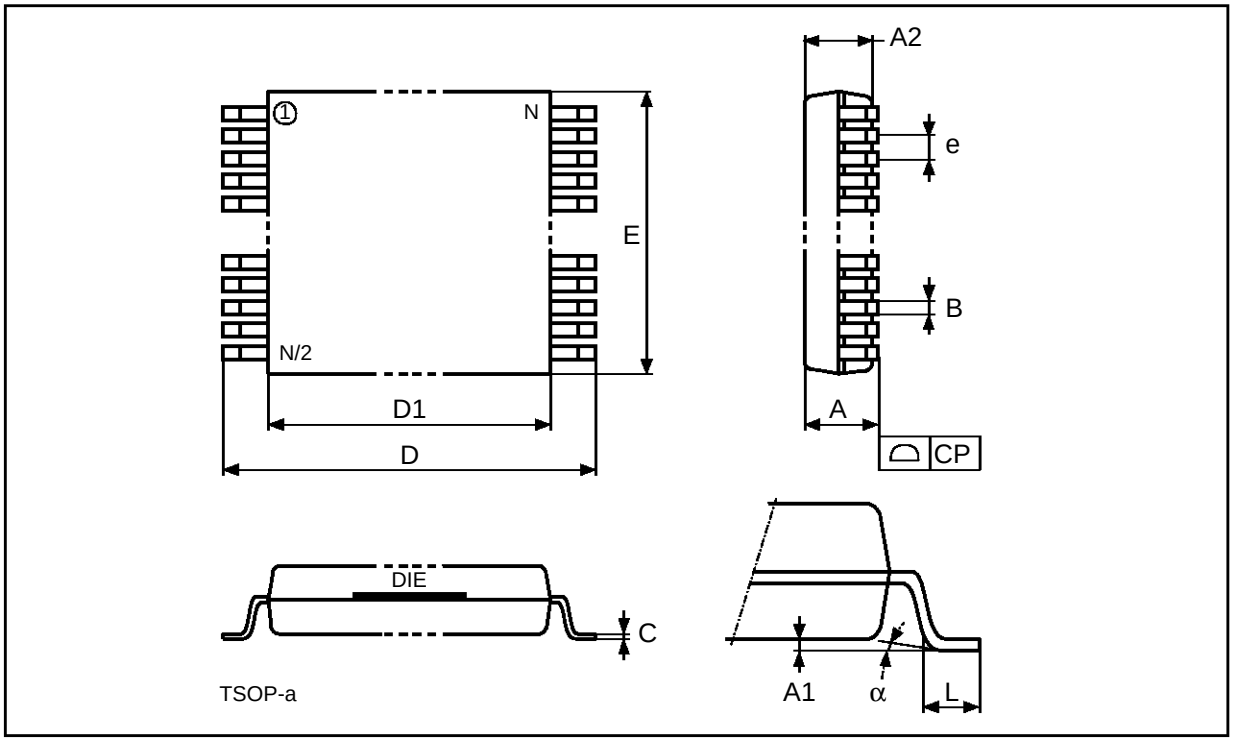
For a list of available options (V_{CC} Range, Array Organisation, Speed, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact SGS-THOMSON Sales Office nearest to you.

TSOP40 Normal Pinout - 40 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	40			40		
CP			0.10			0.004

TSOP40



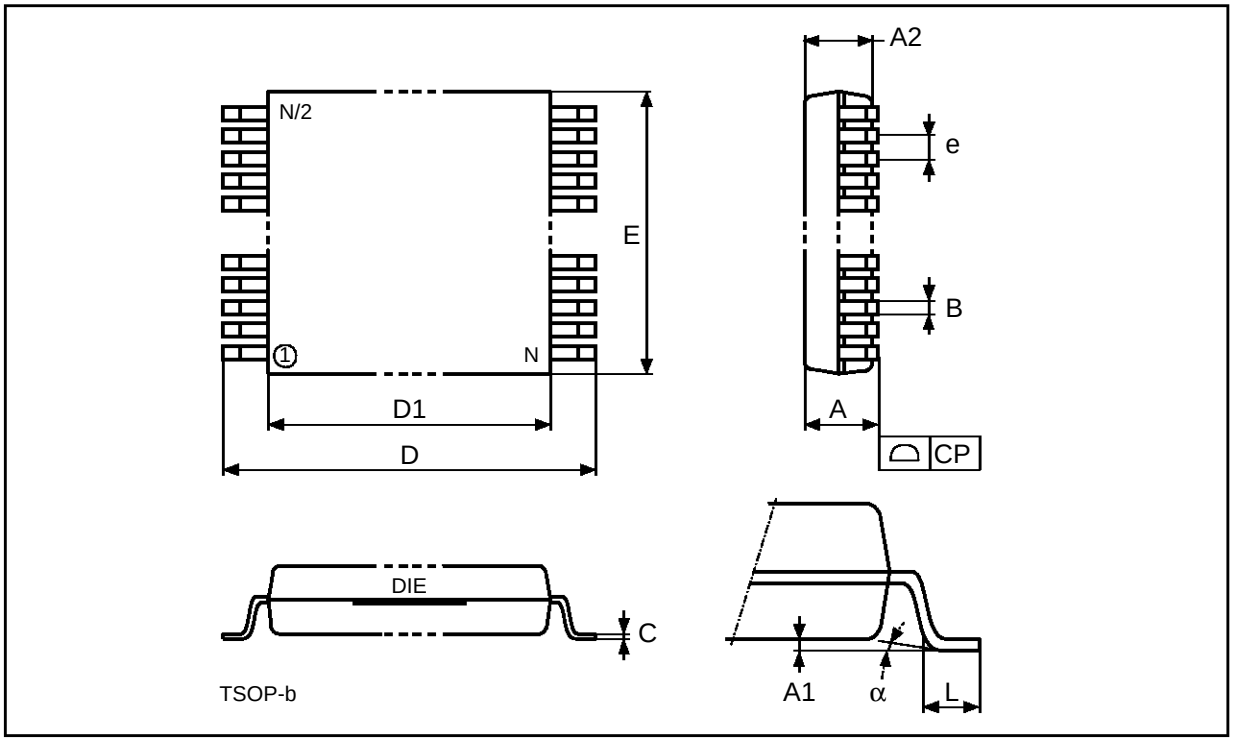
TSOP-a

Drawing is not to scale

TSOP40 Reverse Pinout - 40 lead Plastic Thin Small Outline, 12 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.17	0.27		0.007	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		9.90	10.10		0.390	0.398
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	40			40		
CP			0.10			0.004

TSOP40



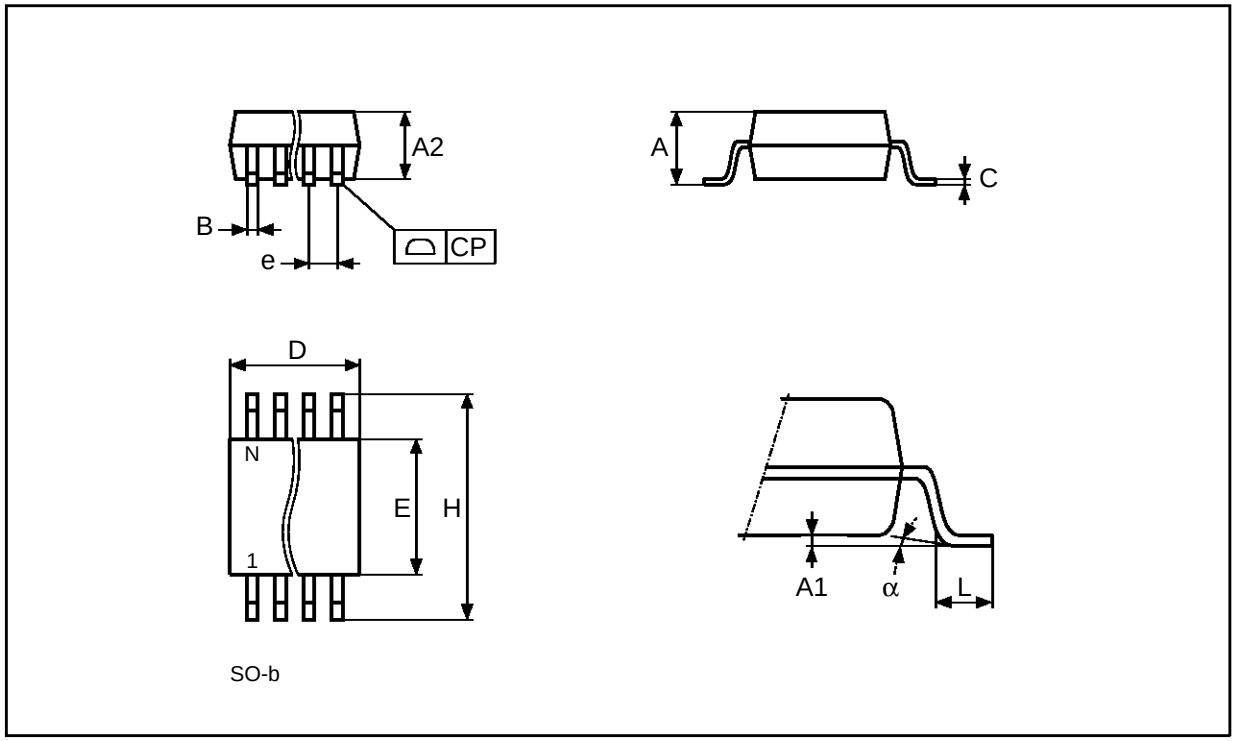
TSOP-b

Drawing is not to scale

SO44 - 44 lead Plastic Small Outline, 525 mils body width

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.42	2.62		0.095	0.103
A1		0.22	0.23		0.009	0.010
A2		2.25	2.35		0.089	0.093
B			0.50			0.020
C		0.10	0.25		0.004	0.010
D		28.10	28.30		1.106	1.114
E		13.20	13.40		0.520	0.528
e	1.27	–	–	0.050	–	–
H		15.90	16.10		0.626	0.634
L	0.80	–	–	0.031	–	–
α	3°	–	–	3°	–	–
N	44			44		
CP			0.10			0.004

SO44



SO-b

Drawing is not to scale